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03/12/18

AMRUPT, SP18

**Goals**

My goals for the week were to meet with Prof. Kan to validate my switch architecture and also work with Russell to discuss the sampling rate of the CC1310. This should allow us to start the project once we have the hardware finalized. I also wanted to restructure the review of literature in response to Julian’s comments from last week. I also wanted to help Russell with his CC1310 I/Q extraction work.

**Problem**

Specifically, I wanted to address the switch architecture. Many people seemed skeptical of the daisy chained switch architecture and also we needed to figure out what switch parameters are necessary in order to have a successful switching architecture. I also wanted to review Russell’s I/Q extraction code.

**General Approach**

The focus of my problem solving this week was meeting with Dr. Kan in order to hear his directional advice on our proposed architecture. This included hearing about recommended literature, switch architecture and thoughts on the CC1310. I also read through the CC1310 datasheets to better understand what Russell is working on. Dr. Kan also agreed that an intelligence approach would be to use a signal generator to emulate the setup to assess performance of the system.

**Planned Course of Action**

This was a very productive week. Dr. Kan confirmed the fact that most switches (including the ones he uses) are 2:1 switches and that this is the correct switching architecture. The diagram in one of his papers which depicted a 4:1 switch confused us a bit, but he clarified saying that was in fact daisy chained switched. A lot of the future work will then depend on what insertion loss and non-linearity we can tolerate. This is something that depends on the chip parameters. Russell will address this in his update, but it seems like we may have to adapt to an SDR to accommodate the frequencies we want to use. Once an SDR or other chip is picked out a switch can be chosen.

1. https://dl.acm.org/citation.cfm?id=2973754

Note: this paper includes the system architecture diagram which includes the switching architecture.

1. <http://www.memtronics.com/files/3%20RF%20MEMS%20Capacitive%20Switches%20MAGWL%201998.pdf>

Note: this paper offers an overview of switch architecture and key performance parameters.